CLAIMS

What is claimed is:

1. A method of configuring a programmable logic device (PLD) comprising a first random access memory (RAM) circuit that includes a first array of rows and columns of RAM cells and a first redundant column of the RAM cells, the method comprising:

initiating a configuration sequence for the PLD;

initiating a built in self test (BIST) procedure on the first array;

setting, when an error associated with the first array is reported by the BIST procedure, a first error flag in a first volatile memory circuit associated with a first defective column of the RAM cells in the first array; and

loading first PLD configuration data into the first RAM circuit, wherein when the first error flag is set the first PLD configuration data bypasses the first defective column of the RAM cells and a first portion of the first PLD configuration data is loaded into the first redundant column of the RAM cells.

2. The method of Claim 1, wherein the PLD comprises a second RAM circuit that includes a second array of rows and columns of the RAM cells and a second redundant column of the RAM cells, the method further comprising:

initiating the BIST procedure on the second array concurrently with initiating the BIST procedure on the first array;

setting, when an error associated with the second array is reported by the BIST procedure, a second error flag in a second volatile memory circuit associated with a second defective column of the RAM cells in the second array; and

loading second PLD configuration data for the PLD into the second RAM circuit, wherein when the second error flag is set the second PLD configuration data bypasses the second defective column of the RAM cells and a second portion of the second PLD configuration data is loaded into the second redundant column of the RAM cells.

3. The method of Claim 1, wherein initiating a configuration sequence for the PLD comprising powering up the PLD.

4. The method of Claim 1, wherein the PLD is a field programmable gate array (FPGA).

5. The method of Claim 1, wherein the first RAM circuit includes a plurality of redundant columns of the RAM cells, and setting the first error flag comprises setting an error flag associated with a defective plurality of columns of the RAM cells.

6. The method of Claim 5, wherein the plurality of redundant columns of the RAM cells are adjacent to one another within the first RAM circuit.

7. The method of Claim 5, wherein the plurality of redundant columns of the RAM cells are organized into groups that are equally spaced from one another within the first RAM circuit.

8. The method of Claim 1, wherein the BIST procedure comprises writing and reading a checkerboard pattern and a reverse checkerboard pattern.

9. The method of Claim 1, wherein the columns of RAM cells comprise linear groupings of the RAM cells oriented along bit lines of the array.

10. The method of Claim 1, wherein the columns of RAM cells comprise linear groupings of the RAM cells oriented along word lines of the array.

11. A programmable logic device (PLD), comprising:

a first read/write data access port;

a first random access memory (RAM) circuit comprising a first array of rows and columns of RAM cells and further comprising a first redundant column of the RAM cells;

a first routing circuit coupled between the first data access port and the first RAM circuit, the first routing circuit comprising a plurality of programmable interconnections between the first data access port and selected columns of the first RAM circuit, the first routing circuit further comprising a plurality of volatile memory circuits coupled to program the programmable routing interconnections;

a built in self test (BIST) control circuit coupled to the volatile memory circuits of the first routing circuit and further coupled to the first RAM circuit;

a configuration data port; and

a configuration control circuit coupled to the BIST control circuit, the configuration data port, and the first RAM circuit.

12. The PLD of Claim 11, further comprising:

a second read/write data access port;

a second RAM circuit comprising a second array of rows and columns of the RAM cells and further comprising a second redundant column of the RAM cells; and

a second routing circuit coupled between the second data access port and the second RAM circuit, the second routing circuit comprising a plurality of programmable interconnections between the second data access port and selected columns of the second RAM circuit, the second routing circuit further comprising a plurality of volatile

memory circuits coupled to program the programmable routing interconnections,

wherein:

the BIST control circuit is further coupled to the volatile memory circuits of the second routing circuit and to the second RAM circuit; and

the configuration control circuit is further coupled to the second RAM circuit.

13. The PLD of Claim 11, wherein the columns of RAM cells comprise linear groupings of the RAM cells oriented along bit lines of the first array.

14. The PLD of Claim 11, wherein the columns of RAM cells comprise linear groupings of the RAM cells oriented along word lines of the first array.

15. A programmable logic device (PLD), comprising:

a first random access memory (RAM) circuit that includes a first array of rows and columns of RAM cells and a first redundant column of the RAM cells;

means for initiating a configuration sequence for the PLD;

means for initiating a built in self test (BIST) procedure on the first array;

means for setting, when an error associated with the first array is reported by the BIST procedure, a first error flag in a first volatile memory circuit associated with a first defective column of the RAM cells in the first array; and

means for loading first PLD configuration data into the first RAM circuit, wherein when the first error flag is set the first PLD configuration data bypasses the first defective column of the RAM cells and a first portion of the first PLD configuration data is loaded into the first redundant column of the RAM cells.

16. The PLD of Claim 15, further comprising:

a second RAM circuit that includes a second array of rows and columns of the RAM cells and a second redundant column of the RAM cells;

means for initiating the BIST procedure on the second array concurrently with initiating the BIST procedure on the first array;

means for setting, when an error associated with the second array is reported by the BIST procedure, a second error flag in a second volatile memory circuit associated with a second defective column of the RAM cells in the second array; and

means for loading second PLD configuration data for the PLD into the second RAM circuit, wherein when the second error flag is set the second PLD configuration data bypasses the second defective column of the RAM cells and a second portion of the second PLD configuration data is loaded into the second redundant column of the RAM cells.

17. The PLD of Claim 15, wherein the means for initiating a configuration sequence for the PLD comprises means for detecting a powering up of the PLD.

18. The PLD of Claim 15, wherein the PLD is a field programmable gate array (FPGA).

19. The PLD of Claim 15, wherein the first RAM circuit includes a plurality of redundant columns of the RAM cells, and the means for setting the first error flag comprises means for setting an error flag associated with a defective plurality of columns of the RAM cells.

20. The PLD of Claim 19, wherein the plurality of redundant columns of the RAM cells are adjacent to one another within the first RAM circuit.

21. The PLD of Claim 19, wherein the plurality of redundant columns of the RAM cells are organized into groups that are equally spaced from one another within the first RAM circuit.

22. The PLD of Claim 15, wherein the BIST procedure comprises writing and reading a checkerboard pattern and a reverse checkerboard pattern.

23. The PLD of Claim 15, wherein the columns of RAM cells comprise linear groupings of the RAM cells oriented along bit lines of the array.

24. The PLD of Claim 15, wherein the columns of RAM cells comprise linear groupings of the RAM cells oriented along word lines of the array.

25. A method of configuring a programmable logic device (PLD) comprising a first random access memory (RAM) circuit that includes a first array of rows and columns of RAM cells and a first redundant column of the RAM cells, the method comprising:

initiating a built in self test (BIST) procedure on the first array;

resuming normal user operation when no errors associated with the first array are reported by the BIST procedure;

setting, when an error associated with the first array is reported by the BIST procedure, a first error flag in a first volatile memory circuit associated with a first defective column of the RAM cells in the first array; and

resuming user operation, when an error associated with the first array is reported by the BIST procedure, while using the first error flag to bypass the first defective column and to shunt read and write data from and to the first redundant column instead of the first defective column.

26. The method of Claim 25, wherein the PLD comprises a second RAM circuit that includes a second array of rows and columns of the RAM cells and a second redundant column of the RAM cells, the method further comprising:

initiating the BIST procedure on the second array concurrently with initiating the BIST procedure on the first array; and

setting, when an error associated with the second array is reported by the BIST procedure, a second error flag in a second volatile memory circuit associated with a second defective column of the RAM cells in the second array,

wherein resuming user operation, when an error associated with the second array is reported by the BIST procedure, comprises using the second error flag to bypass the second defective column and to shunt read and write data from and to the second redundant column instead of the second defective column.

27. The method of Claim 25, wherein the PLD is a field programmable gate array (FPGA).

28. The method of Claim 25, wherein the first RAM circuit includes a plurality of redundant columns of the RAM cells, and setting the first error flag comprises setting an error flag associated with a defective plurality of columns of the RAM cells.

29. The method of Claim 28, wherein the plurality of redundant columns of the RAM cells are adjacent to one another within the first RAM circuit.

30. The method of Claim 28, wherein the plurality of redundant columns of the RAM cells are organized into groups that are equally spaced from one another within the first RAM circuit.

31. The method of Claim 25, wherein the BIST procedure comprises writing and reading a checkerboard pattern and a reverse checkerboard pattern.

32. The method of Claim 25, wherein the columns of RAM cells comprise linear groupings of the RAM cells oriented along bit lines of the array.

33. The method of Claim 25, wherein the columns of RAM cells comprise linear groupings of the RAM cells oriented along word lines of the array.

34. A programmable logic device (PLD), comprising:

a first random access memory (RAM) circuit that includes a first array of rows and columns of RAM cells and a first redundant column of the RAM cells;

means for initiating a built in self test (BIST) procedure on the first array;

means for resuming normal user operation when no errors associated with the first array are reported by the BIST procedure;

means for setting, when an error associated with the first array is reported by the BIST procedure, a first error flag in a first volatile memory circuit associated with a first defective column of the RAM cells in the first array; and

means for resuming user operation, when an error associated with the first array is reported by the BIST procedure, while using the first error flag to bypass the first defective column and to shunt read and write data from and to the first redundant column instead of the first defective column.

35. The PLD of Claim 34, further comprising:

a second RAM circuit that includes a second array of rows and columns of the RAM cells and a second redundant column of the RAM cells;

means for initiating the BIST procedure on the second array concurrently with initiating the BIST procedure on the first array; and

means for setting, when an error associated with the second array is reported by the BIST procedure, a second error flag in a second volatile memory circuit associated with a second defective column of the RAM cells in the second array,

wherein the means for resuming user operation comprises means for, when an error associated with the second array is reported by the BIST procedure, using the second error flag to bypass the second defective column and to shunt read and write data from and to the second redundant column instead of the second defective column.

36. The PLD of Claim 34, wherein the PLD is a field programmable gate array (FPGA).

37. The PLD of Claim 34, wherein the first RAM circuit includes a plurality of redundant columns of the RAM cells, and the means for setting the first error flag comprises means for setting an error flag associated with a defective plurality of columns of the RAM cells.

38. The PLD of Claim 37, wherein the plurality of redundant columns of the RAM cells are adjacent to one another within the first RAM circuit.

39. The PLD of Claim 37, wherein the plurality of redundant columns of the RAM cells are organized into groups that are equally spaced from one another within the first RAM circuit.

40. The PLD of Claim 34, wherein the BIST procedure comprises writing and reading a checkerboard pattern and a reverse checkerboard pattern.

41. The PLD of Claim 34, wherein the columns of RAM cells comprise linear groupings of the RAM cells oriented along bit lines of the array.

42. The PLD of Claim 34, wherein the columns of RAM cells comprise linear groupings of the RAM cells oriented along word lines of the array.